Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor memory device driven by a first power supply potential and a second power supply potential supplied independently from each other and a reference potential, the second power supply potential being different from the first power supply potential, comprising:

a memory array including a plurality of memory cells arranged in a plurality of rows and a plurality of columns, a plurality of word lines provided corresponding to said plurality of rows, respectively, and a plurality of sets of first and second bit lines provided corresponding to said plurality of columns, respectively;

a sense amplifier provided corresponding to each set of the first and the second bit lines to amplify a potential difference generated between corresponding bit lines to a potential difference between said first power supply potential and said reference potential;

a row decoder to select one word line from said plurality of word lines according to a row address signal and to activate each memory cell corresponding to the selected word line;

first and second read data lines provided commonly to said plurality of sets of first and second bit lines and previously charged to said second power supply potential;

first and second write data lines commonly provided for said plurality of sets of first and second bit lines;

a plurality of read column select lines and write column select lines provided corresponding to said plurality of sets of first and second bit lines, respectively;

a read column decoder to select one read column select line from said plurality of read column select lines according to a column address signal and to turn the selected read column select line to said second power supply potential at a reading operation;

a write column decoder to select one write column select line from said plurality of write column select lines according to a column address signal and to turn the selected write column select line to said first power supply potential at a writing operation;

a read column select gate provided corresponding to each set of the first and the second bit lines, in response to an attainment of said second power supply potential by a corresponding read column select line through said read column decoder, to transmit a potential difference of a corresponding set of first and second bit lines to said first and second read data lines;

a read circuit to read a data signal of a memory cell selected by said row decoder and said column decoder based on a potential difference of said first and second read data lines;

a write circuit to turn one write data line of said first and second write data lines to said second power supply potential and to turn another write data line to said reference potential according to an external data signal; and

a write column select gate provided corresponding to each set of the first and the second bit lines, in response to an attainment of said first power supply potential by a corresponding write column select line through said write column decoder, to transmit a potential difference of said first and second write data lines to a corresponding set of first and second bit lines; wherein

said read column select gate includes

first and second transistors, connected in series between said first read data line and a line of said reference potential and a gate electrode of one transistor of said first and second transistors is connected to a corresponding first bit line and a gate electrode of another transistor of said first and second transistors is connected to a corresponding read column select line, and

third and fourth transistors, connected in series between said second read data line and the line of said reference potential, a gate electrode of one transistor of said third and fourth transistors is connected to a corresponding second bit line and a gate electrode of another transistor is connected to a corresponding read column select line;

said write column select gate includes

fifth and sixth transistors connected in series between a corresponding first bit line and a line of said reference potential, a gate electrode of one transistor of said fifth and sixth transistors is connected to a corresponding write column select line and a gate electrode of another transistor of said fifth and sixth transistors is connected to said first write data line, and

seventh and eighth transistors connected in series between a corresponding second bit line and the line of said reference potential, a gate electrode of one transistor of said seventh and eighth transistors is connected to a corresponding write column select line and a gate electrode of another transistor of said seventh and eighth transistors is connected to said second write data line.

2. (Currently Amended) A semiconductor memory device driven by a first power supply potential and a second power supply potential supplied independently from each other and a reference potential, the second power supply potential being different from the first power supply potential, comprising:

a memory array including a plurality of memory cells arranged in a plurality of rows and a plurality of columns, a plurality of word lines provided corresponding to said plurality of rows, respectively, and a plurality of sets of first and second bit lines provided corresponding to said plurality of columns, respectively;

a sense amplifier provided corresponding to each set of the first and the second bit lines to amplify a potential difference generated between corresponding bit lines to a potential difference between said first power supply potential and said reference potential;

a row decoder to select one word line from said plurality of word lines according to a row address signal and to activate each memory cell corresponding to the selected word line;

first and second read data lines provided commonly to said plurality of sets of first and second bit lines and previously charged to said second power supply potential;

first and second write data lines commonly provided for said plurality of sets of first and second bit lines;

a plurality of read column select lines and write column select lines provided corresponding to said plurality of sets of first and second bit lines, respectively;

a read column decoder to select one read column select line from said plurality of read column select lines according to a column address signal and to turn the selected read column select line to said second power supply potential at a reading operation;

a write column decoder to select one write column select line from said plurality of write column select lines according to a column address signal and to turn the selected write column select line to said first power supply potential at a writing operation;

a read column select gate provided corresponding to each set of the first and the second bit lines, in response to an attainment of said second power supply potential by the corresponding read column select line through said read column decoder, to transmit a potential difference of the corresponding set of first and second bit lines to said first and second read data lines;

a read circuit to read a data signal of a memory cell selected by said row decoder and said column decoder based on a potential difference of said first and second read data lines;

a write circuit to turn one write data line of said first and second write data lines to said second power supply potential and to turn another write data line to said reference potential according to an external data signal; and

a write column select gate provided corresponding to each set of the first and the second bit lines, activated when a write mask signal is at said second power supply potential, in response to an attainment of said first power supply potential by a corresponding write column select line through said write column decoder, to transmit a potential difference between said first and second write data lines to a corresponding set of first and second bit lines; wherein

said read column select gate includes

first and second transistors, connected in series between said first read data line and a line of said reference potential and a gate electrode of one transistor of said first and second transistors is connected to a corresponding first bit line and a gate electrode of another transistor of said first and second transistors is connected to a corresponding read column select line, and

third and fourth transistors, connected in series between said second read data line and the line of said reference potential, a gate electrode of one transistor of said third and fourth transistors is connected to a corresponding second bit line and a gate electrode of another transistor is connected to a corresponding read column select line;

said write column select gate includes

fifth and sixth transistors connected in series between a corresponding first bit line and said first write data line, a gate electrode of one transistor of said fifth and sixth transistors receives said write mask signal, and a gate electrode of another transistor of said fifth and sixth transistors is connected to said write column select line, and

seventh and eighth transistors connected in series between a corresponding second bit line and said second write data line, a gate electrode of one transistor of said seventh and eighth transistors receives said write mask signal and a gate electrode of another transistor of said seventh and eighth transistors is connected to said write column select line.

3. (Currently Amended) A semiconductor memory device driven by a first power supply potential and a second power supply potential supplied independently from each other and a reference potential, the second power supply potential being different from the first power supply potential, comprising:

a memory array including a plurality of memory cells arranged in a plurality of rows and a plurality of columns, a plurality of word lines provided corresponding to said plurality of rows, respectively, and a plurality of sets of first and second bit lines provided corresponding to said plurality of columns, respectively;

a sense amplifier provided corresponding to each set of the first and the second bit lines to amplify a potential difference generated between corresponding bit lines to a potential difference between said first power supply potential and said reference potential;

a row decoder to select one word line from said plurality of word lines according to a row address signal and to activate each memory cell corresponding to the selected word line;

first and second data lines commonly provided for said plurality of sets of first and second bit lines;

a plurality of sets of first and second column select lines provided corresponding to said plurality of sets of first and second bit lines, respectively;

a [[row]] column decoder to select one set of first and second column select lines from said plurality of sets of first and second column select lines according to a column address signal and to turn the selected first and second column select lines to said first and second power supply potential, respectively;

a column select gate provided corresponding to each set of the first and the second bit lines, in response to an attainment of said first and second power supply potential by a corresponding first and second column select lines through said column decoder, respectively, to connect a corresponding first bit line and said first data line and to connect a corresponding second bit line and said second data line; and

a read/write circuit connected to said first and second data lines to read/write a data signal of a memory cell selected by said row decoder and said column decoder; wherein

said column select gate includes

first and second transistors connected in series between a corresponding first bit line and said first data line, a gate electrode of one transistor of said first and second transistors is connected to said first column select line and a gate electrode of another transistor of said first and second transistors is connected to said second column select line, and

third and fourth transistors connected in series between a corresponding second bit line and said second data line, a gate electrode of one transistor of said third and fourth transistors is connected to said first column select line and a gate electrode of another transistor of said third and fourth transistors is connected to said second column select line.

4. (Original) The semiconductor memory device according to claim 3, wherein said read/write circuit, at a write mask operation prohibiting data overwriting of said memory cell, turns each of said first and second data lines to said second power supply potential.